IN THE CLAIMS

Please amend the claims as follows:

Claims 1-9 (Canceled).

Claim 10 (Currently Amended): ~~The processor according to Claim 1, wherein~~ A processor, comprising:

a processor core for executing an instruction in a pipeline processing;

a data memory accessed by said processor core; and

an extended arithmetic unit, connected to an exterior of said processor core, for processing an extended instruction decoded in said processor core in the pipeline processing,

said extended arithmetic unit executing an arithmetic operation by using arithmetic operation data retained in a register file in said processor core, and outputting a result of an arithmetic operation directly to a pipeline stage processing after an executing stage processing in said processor core,

said processor core receiving the result of the arithmetic operation executed by said extended arithmetic unit and inputted therefrom into said register file in said processor core, wherein said processor core includes a pipeline controller for flushing or stopping the pipeline processing in said extended arithmetic unit, and

said extended arithmetic unit ~~comprises~~[[:]] further comprising

a first stage arithmetic circuit[[;]],

a second stage arithmetic circuit[[;]], and

a memory access controller configured to control direct access of said data memory by the extended arithmetic unit after an execution of the arithmetic operation by said first stage arithmetic circuit, and to provide said second stage arithmetic circuit with read out data from said data memory as input data for succeeding pipeline processing.

Claims 11-19 (Canceled).

Claim 20 (Currently Amended): A processor, comprising:

a processor core having a register file and configured to execute an instruction in a pipeline processing;

a data memory accessed by said processor core;

an extended arithmetic unit connected to an exterior of said processor core and configured to process an extended instruction decoded in said processor core in the pipeline processing, to execute an arithmetic operation by using arithmetic operation data retained in a register file in said processor core, and to output a result of an arithmetic operation directly to a ~~memory~~ pipeline stage processing after an executing stage processing in said processor core;

said processor core configured to receive the result of the arithmetic operation executed by said extended arithmetic unit and to input the received result into said register file in said processor core;

said processor core comprising a pipeline controller configured to flush or stop the pipeline processing in said extended arithmetic unit; and

said extended arithmetic unit comprises,

a first stage arithmetic circuit,

a second stage arithmetic circuit, and

a memory access controller configured to control direct access of said data memory by the extended arithmetic unit after an execution of the arithmetic operation by said first stage arithmetic circuit, and to provide said second stage arithmetic circuit with read out data from said data memory as input data for succeeding pipeline processing.

Claim 21 (New): The processor according to claim 10, wherein,

in case that the instruction decoded is said extended instruction, said processor core outputs to said extended arithmetic unit at least an instruction code that specifies an action involved in an arithmetic operation in said extended arithmetic unit and an instruction valid signal that indicates said instruction code is valid.

Claim 22 (New): The processor according to claim 10, wherein said arithmetic operation data outputted to said extended arithmetic unit is a value read out from said register file in said processor core in accordance with a register number specified by a part of said extended instruction.

Claim 23 (New): The processor according to claim 10, wherein said pipeline controller controls pipeline processing in an interior of said processor core and in said extended arithmetic unit.

Claim 24 (New): The processor according to claim 10, wherein said pipeline controller outputs to said extended arithmetic unit a first pipeline stop signal for stopping the pipeline processing in said extended arithmetic unit.

Claim 25 (New): The processor according to claim 10, wherein said pipeline controller, in case that the instruction decoded is a jump instruction, outputs to said extended arithmetic unit a pipeline flush signal for flushing a register in said extended arithmetic unit.

Claim 26 (New): The processor according to claim 10, wherein said extended arithmetic unit further comprises second pipeline controller for, in case that the extended

instruction requires more than one cycle, asserting a second pipeline stop signal for stopping the pipeline processing in said processor core.

Claim 27 (New): The processor according to claim 10, wherein said extended arithmetic unit outputs to said processor core an arithmetic operation result invalidating signal that invalidates an execution result of an arithmetic operation executed in said processor core.

Claim 28 (New): The processor according to claim 10, wherein said extended arithmetic unit includes:

a plurality of pipeline-structured arithmetic circuits;

a first pipeline register for storing a processing result by an arithmetic circuit in a preceding stage at a rising of a following clock; and

a second pipeline register for storing a processing result by an arithmetic circuit in a succeeding stage at the rising of the following clock.

Claim 29 (New): The processor according to claim 20, wherein,

in case that the instruction decoded is said extended instruction, said processor core outputs to said extended arithmetic unit at least an instruction code that specifies an action involved in an arithmetic operation in said extended arithmetic unit and an instruction valid signal that indicates said instruction code is valid.

Claim 30 (New): The processor according to claim 20, wherein said arithmetic operation data outputted to said extended arithmetic unit is a value read out from said register

file in said processor core in accordance with a register number specified by a part of said extended instruction.

Claim 31 (New): The processor according to claim 20, wherein said pipeline controller controls pipeline processing in an interior of said processor core and in said extended arithmetic unit.

Claim 32 (New): The processor according to claim 20, wherein said pipeline controller outputs to said extended arithmetic unit a first pipeline stop signal for stopping the pipeline processing in said extended arithmetic unit.

Claim 33 (New): The processor according to claim 20, wherein said pipeline controller, in case that the instruction decoded is a jump instruction, outputs to said extended arithmetic unit a pipeline flush signal for flushing a register in said extended arithmetic unit.

Claim 34 (New): The processor according to claim 20, wherein said extended arithmetic unit further comprises second pipeline controller for, in case that the extended instruction requires more than one cycle, asserting a second pipeline stop signal for stopping the pipeline processing in said processor core.

Claim 35 (New): The processor according to claim 20, wherein said extended arithmetic unit outputs to said processor core an arithmetic operation result invalidating signal that invalidates an execution result of an arithmetic operation executed in said processor core.

Claim 36 (New): The processor according to claim 20, wherein said extended arithmetic unit includes:

a plurality of pipeline-structured arithmetic circuits;

a first pipeline register for storing a processing result by an arithmetic circuit in a preceding stage at a rising of a following clock; and

a second pipeline register for storing a processing result by an arithmetic circuit in a succeeding stage at the rising of the following clock.